WHAT IS CLAIMED IS:

1. A trenched field effect transistor comprising:

a semiconductor substrate;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions, positioned on opposite sides of the trench;

a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trench, and

a doped well surrounding the heavy body beneath the heavy body.

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

3. The trenched field effect transistor of claim 1 wherein the depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field when voltage is applied to the transistor will be spaced from the trench.

4. The trenched field effect transistor of claim 1 wherein said doped well has a depth less than the predetermined depth of said trench.

5. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

6. The trenched field effect transistor of claim 1 wherein there is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field when voltage is applied to the transistor to occur in the area of the interface.

7. The trenched field effect transistor of claim 6 wherein said abrupt junction has a sheet resistance profile substantially as shown in Fig. 5.

8. An array of transistor cells comprising:

a semiconductor substrate;

a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a

contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches;

surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench;

positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches;

a doped well surrounding each heavy body beneath the heavy body; and

p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

9. The array of transistor cells of claim 8, wherein each said doped well has a substantially flat bottom.

10. The array of transistor cells of claim 8 wherein the depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field when voltage is applied to the transistor will occur approximately halfway between adjacent gate-forming trenches.

11. The array of transistor cells of claim 8 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.

12. The array of transistor cells of claim 8 wherein each said gate-forming trench has rounded top and bottom corners.

13. The array of transistor cells of claim 8 wherein there is an abrupt junction at each interface between the heavy body and the well, to cause the peak electric field when voltage is applied to the transistor to occur in the area of the interface.

14. The array of transistor cells of claim 8 further comprising a field termination structure surrounding the periphery of the array.

15. The array of transistor cells of claim 14 wherein said field termination structure comprises a well having a depth greater than that of the gate-forming trenches.

16. The array of transistor cells of claim 14 wherein said field termination structure comprises a termination trench extending continuously around the periphery of the array.

17. The array of transistor cells of claim 16 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

18. A semiconductor die comprising:

a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and

surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

19. The semiconductor die of claim 18 wherein said field termination structure comprises a doped well.

20. The semiconductor die of claim 18 wherein said field termination structure comprises a termination trench.

21. The semiconductor die of claim 20 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

22. The semiconductor die of claim 18 wherein each of said DMOS transistor cells further comprises a doped heavy body and said doped heavy body extends into said semiconductor substrate to a depth that is less than the predetermined depth of said gate-forming trenches.

23. A method of making a heavy body structure for a trenched DMOS transistor comprising:

providing a semiconductor substrate;

implanting into a region of the substrate a first dopant at a first energy and dosage; and

subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

24. The method of claim 23 wherein said first and second dopants both comprise boron.

25. The method of claim 23 wherein said first energy is from about 150 to 200 keV.

26. The method of claim 25 wherein said first dosage is from about 1E15 to 5E15.

27. The method of claim 23 wherein said second energy is from about 20 to 40 keV.

28. The method of claim 27 wherein said second dosage is from about 1El4 to 1E15.

29. A method of making a source for a trenched DMOS transistor comprising:

providing a semiconductor substrate;

implanting into a region of the substrate a first dopant at a first energy and dosage; and

subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

30. The method of claim 29 wherein said first dopant comprises arsenic and said second dopant comprises phosphorus.

31. The method of claim 29 wherein said first energy is from about 80 to 120 keV.

32. The method of claim 29 wherein said first dosage is from about 5E15 to 1E16.

33. The method of claim 29 wherein said second energy is from about 40 to 70 keV.

34. The method of claim 33 wherein said second dosage is from about 1E15 to 5E15.

35. The method of claim 29 wherein the resulting depth of said source is from about 0.4 to 0.8 μm in the finished DMOS transistor.

36. A method of manufacturing a trenched field effect transistor comprising:

forming a field termination junction around the perimeter of a semiconductor substrate;

forming an epitaxial layer on the semiconductor substrate; patterning and etching a plurality of trenches into the epitaxial layer; depositing polysilicon to fill the trenches;

doping the polysilicon with a dopant of a first type;

patterning the substrate and implanting a dopant of a second, opposite type to form a plurality of wells interposed between adjacent trenches;

patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well;

patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and

applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

37. The method of manufacturing a trenched field effect transistor of claim 36, wherein the trenches are patterned to extend in one direction and be substantially parallel to each other.

38. The method of manufacturing a trenched field effect transistor of claim 36, wherein the patterning and implanting steps further comprise arranging the first dopant type contact areas and second dopant type contact areas in alternation and extend linearly between adjacent trenches.

39. The method of manufacturing a trenched field effect transistor of claim 36, wherein the implanting step for forming the heavy bodies comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

40. The method of manufacturing a trenched field effect transistor of claim 36, wherein the implanting step for forming the source regions comprises implanting a first dopant at a first energy and dosage and a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

41. The method of manufacturing a trenched field effect transistor of claim 36, wherein the heavy bodies are formed prior to forming the source regions.

42. The method of manufacturing a trenched field effect transistor of claim 36 wherein the source regions are formed prior to the heavy bodies.

43. The method of manufacturing a trenched field effect transistor of claim 36 wherein said field termination is formed by forming a trench ring.

44. The method of manufacturing a trenched field effect transistor of claim 36 wherein said field termination is formed by forming a deep well doped with a dopant of the second dopant type.

45. The method of manufacturing a trenched field effect transistor of claim 36 wherein said dielectric is applied before the steps of forming the heavy bodies and second dopant type contacts, and the dielectric provides a mask for the patterning of the heavy bodies and second dopant type contacts.